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| 10/670,840 | 09/25/2003 | Michael Norman Day | AUS920030718US1 | 1485 |

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| EXAMINER | |
|---|---|
| KROFCHECK, MICHAEL C | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2186 | |

DATE MAILED: 10/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/670,840 | DAY ET AL. | |
| | Examiner | Art Unit | |
| | Michael Krofcheck | 2186 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *26 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-7,9-16,18-25 and 27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-16,18-25 and 27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/16, 8/15, 9/19*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. This office action is in response to the amendment filed on 7/26/2006.

2. Claims 1. 10, and 19 have been amended.

3. The objections/rejections from the prior correspondence not restated herein have been withdrawn.

### *Claim Rejections - 35 USC § 103*

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1 – 6, 10-15 and 19-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuoki at al U.S. Patent No. 6,526,491 (hereinafter Suzuoki), an admission of prior art by the applicant, Pfleiger et al., US patent application publication 2004/0260685, and Hammond, US patent 4787057.

7. With respect to claim 1, Suzuoki teaches of a computer-implemented method for handling data using a plurality of processors, the method comprising: dividing a common memory, accessible to one or more first processors and to one or more secondary processors, into a plurality of data blocks using one of the first processors (figs. 2, 24; item 2412; column 3, lines 43 – 53; column 7, lines 43 – 56; column 18, lines 32 – 35; where the processing unit allocates space in the DRAM for executing the apulet by issuing a DMA command to the DMAC to setup the necessary sandboxes. The sandboxes are exclusive areas in the DRAM which only a specific attached processing unit can access),

identifying an available processor from the secondary processors to process one of the data blocks (fig. 24; item 2410; column 7, lines 57 – 66; column 18, lines 31 – 32; where the processing unit designates an attached processing unit to process the apulet);

and processing the data block using the available secondary processor (fig. 24; item 2438; column 7, lines 57 – 66; column 18, lines 66 – 67; where the attached processing unit processes the apulet and generates a result).

The applicant admits as prior art that the one or more first processors and the one or more second processors being chosen from a group of heterogeneous processors (applicant's specification page 1, lines 12 – 19; where the multiple processors are dissimilar, with each processor specializing in a particular processing task).

Pfleiger teaches of processing the data block further using one of the first processors (paragraph 0002; where the processor combines all the individual results from each execution engine to form a complete result)

Hammond teaches of wherein each of the data blocks includes a plurality of coefficients corresponding to a plurality of linear equations (column 3, line 51-column 4, line 9; it is abundantly clear to one of ordinary skill in the art that the values in the matrices are coefficients for the linear equations as that is how simple linear equations are evaluated by hand),

the processing resulting in one or more solutions to one or more of the plurality of linear equations (column 3, lines 47-51).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have the multiple processors (PUs and APUs) in Suzuoki be different as is admitted prior art by the applicant. Suzuoki expresses the desire for the network to include a multitude of different computing devices, such as PCs, PDAs, appliances, and others (column 2, lines 61 – 64). To accomplish this, having multiple processors that are dissimilar, that is each processor specializing in a specific task, is necessary.

It would have been obvious to one of ordinary skill in the art having the teachings of Suzuoki, and applicants admission and Pfleiger at the time of the invention to have the PU of Suzuoki combine the results from the individual APU for the distributed task as taught in Pfleiger. Their motivation would have been to provide a single overall result (Pfleiger, paragraph 0002).

It would have been obvious to one of ordinary skill in the art having the teachings of Suzuoki, applicants admission, Pfleiger, and Hammond at the time of the invention to evaluate linear equations in the combination of Suzuoki, AAPA, and Pfleiger as taught in Hammond. Their motivation would have been to increase the efficiency and lower the cost of processing linear equations (Hammond, column 4, lines 39-55).

8. With respect to claim 2, Suzuoki also teaches of directly accessing the data block in the common memory using a memory access unit of the available secondary processor (fig. 17E; item 1742; column 13, lines 9 – 18; where the control logic issues a command which reads a memory location in the DRAM).

9. With respect to claim 3, Suzuoki also teaches of transferring the data block using the available secondary processor from the common memory to a secondary memory local to the available secondary processor (figs. 17G, 24; items 2434, 2436; column 13, lines 19 – 21; column 18, lines 61 – 66; where the data is read from the DRAM into the local storage of the attached processing unit).

10. With respect to claim 4, Suzuoki also teaches of transferring the data block using the available secondary processor from the secondary memory to the common memory after processing the data block (fig. 24; items 2440, 2442; column 18, line 67 – column 19, line 4; where the APU issues a DMA command to store the result in the DRAM from the APU's local memory).

11. With respect to claim 5, Suzuoki also teaches of the available secondary processor notifying one of the first processors after processing the data block (fig. 24;

item 2444; column 19, line 4 – 6; where the APU issues an interrupt request to the PU to signal that the processing is complete).

12. With respect to claim 6, Suzuoki also teaches of requesting, using one of the first processors, the secondary processor to process the data block (fig. 24; item 2410; column 18, lines 31 – 32; where the processing unit designates an APU to process the apulet).

13. With respect to claim 10 Suzuoki teaches of an information handling system comprising a plurality of processors (figs. 2, 3; column 7, lines 19 – 25),

wherein the plurality of processors comprises one or more first processors and one or more secondary processors (figs. 2, 3; column 7, lines 19 – 25; column 8, lines 9 – 10; where the processors comprise processing units, PUs (first processors) and attached processing units, APUs (secondary processors));

and a common memory accessible by the plurality of processors (figs. 2, 3; items 225, 315; column 7, lines 42 – 52; where the DRAM is accessed by the processors, PU and APU alike),

wherein one of the first processors is adapted to divide the common memory into a plurality of data blocks (figs. 2, 24; item 2412; column 3, lines 43 – 53; column 7, lines 43 – 56; column 18, lines 32 – 35; where the processing unit allocates space in the DRAM for executing the apulet by issuing a DMA command to the DMAC to setup the necessary sandboxes. The sandboxes are exclusive areas in the DRAM which only a specific attached processing unit can access),

one of the first processors is adapted to identify an available processor from the secondary processors to process one of the data block (fig. 24; item 2410; column 7, lines 57 – 66; column 18, lines 31 – 32; where the processing unit designates an attached processing unit to process the apulet);

and one of the secondary processors is adapted to process the data block (fig. 24; item 2438; column 7, lines 57 – 66; column 18, lines 66 – 67; where the attached processing unit processes the apulet and generates a result).

The applicant's admitted prior art teaches of a plurality of heterogeneous processors (applicant's specification page 1, lines 12 – 19; where the multiple processors are dissimilar, with each processor specializing in a particular processing task).

Pfleiger teaches of wherein one of the first processors is adapted to further process the data block (paragraph 0002).

Hammond teaches of wherein each of the data blocks includes a plurality of coefficients corresponding to a plurality of linear equations (column 3, line 51-column 4, line 9; it is abundantly clear to one of ordinary skill in the art that the values in the matrices are coefficients for the linear equations as that is how simple linear equations are evaluated by hand),

the processing resulting in one or more solutions to one or more of the plurality of linear equations (column 3, lines 47-51).

14. With respect to claim 11, Suzuoki also teaches of wherein the available secondary processor is further adapted to directly access the data block in the common

memory using a memory access unit (fig. 17E; item 1742; column 13, lines 9 – 18; where the control logic issues a command which reads a memory location in the DRAM).

15. With respect to claim 12, Suzuoki also teaches of wherein the available secondary processor is further adapted to transfer the data block from the common memory to a secondary memory local to the available secondary processor (figs. 17G, 24; items 2434, 2436; column 13, lines 19 – 21; column 18, lines 61 – 66; where the data is read from the DRAM into the local storage of the attached processing unit).

16. With respect to claim 13,. Suzuoki also teaches of wherein the available secondary processor is further adapted to transfer the data block from the secondary memory to the common memory after processing the data block (fig. 24; items 2440, 2442; column 18, line 67 – column 19, line 4; where the APU issues a DMA command to store the result in the DRAM from the APU's local memory).

17. With respect to claim 14, Suzuoki also teaches of wherein the available secondary processor is further adapted to notify one of the first processors after processing the data block (fig. 24; item 2444; column 19, line 4 – 6; where the APU issues an interrupt request to the PU to signal that the processing is complete).

18. With respect to claim 15, Suzuoki also teaches of wherein one of the first processors is adapted to request the available secondary processor to process the data block (fig. 24; item 2410; column 18, lines 31 – 32; where the processing unit designates an APU to process the apulet).

19. With respect to claim 19, Suzuoki teaches of a computer program product on computer operable media, the computer program product comprising: means for dividing a common memory, accessible to one or more first processors and to one or more secondary processors, into a plurality of data blocks (figs. 2, 24; item 2412; column 3, lines 43 – 53; column 7, lines 43 – 56; column 18, lines 32 – 35; where the processing unit allocates space in the DRAM for executing the apulet by issuing a DMA command to the DMAC to setup the necessary sandboxes. The sandboxes are exclusive areas in the DRAM which only a specific attached processing unit can access),

means for identifying an available processor from the secondary processors to process one of the data blocks (fig. 24; item 2410; column 7, lines 57 – 66; column 18, lines 31 – 32; where the processing unit designates an attached processing unit to process the apulet); and

means for processing the data block using the available secondary processor (fig. 24; item 2438; column 7, lines 57 – 66; column 18, lines 66 – 67; where the attached processing unit processes the apulet and generates a result).

The applicant's admitted prior art teaches of wherein the one or more first processors and the one or more second processors are selected from a group of heterogeneous processors (applicant's specification page 1, lines 12 – 19; where the multiple processors are dissimilar, with each processor specializing in a particular processing task).

Pfleiger teaches of means for processing the data block further (paragraph 0002).

Hammond teaches of wherein each of the data blocks includes a plurality of coefficients corresponding to a plurality of linear equations (column 3, line 51-column 4, line 9; it is abundantly clear to one of ordinary skill in the art that the values in the matrices are coefficients for the linear equations as that is how simple linear equations are evaluated by hand),

the processing resulting in one or more solutions to one or more of the plurality of linear equations (column 3, lines 47-51).

20. With respect to claim 20, Suzuoki also teaches of means for directly accessing the data block in the common memory (fig. 17E; item 1742; column 13, lines 9 – 18; where the control logic issues a command which reads a memory location in the DRAM).

21. With respect to claim 21, Suzuoki also teaches of means for transferring the data block from the common memory to a secondary memory local to the available secondary processor (figs. 17G, 24; items 2434, 2436; column 13, lines 9 – 21; column 18, lines 61 – 66; where the control unit issues a command to read the data in a memory location in the DRAM and subsequently, the data is read from the DRAM into the local storage of the attached processing unit).

22. With respect to claim 22, Suzuoki also teaches of means for transferring the data block from the secondary memory to the common memory after processing the data

block (fig. 24; items 2440, 2442; column 18, line 67 – column 19, line 4; where the APU issues a DMA command to store the result in the DRAM from the APU's local memory).

23. With respect to claim 23, Suzuoki also teaches of means for notifying one of the first processors after processing the data block (fig. 24; item 2444; column 19, line 4 – 6; where the APU issues an interrupt request to the PU to signal that the processing is complete).

24. With respect to claim 24, Suzuoki also teaches of means for requesting the secondary processor to process the data block (fig. 24; item 2410; column 18, lines 31 – 32; where the processing unit designates an APU to process the apulet).

25. Claims 7, 16, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuoki, the applicant's admitted prior art, Pfleiger and Hammond as applied to claims 1, 10, and 19 respectively, and further in view of Lee et al., U.S. Patent No. 6,128,724 (hereinafter Lee).

26. With respect to claim 7, Suzuoki teaches of wherein the dividing comprises dividing the common memory into data blocks (figs. 2, 24; item 2412; column 3, lines 43 – 53; column 7, lines 43 – 56; column 18, lines 32 – 35; where the processing unit allocates space in the DRAM for executing the apulet by issuing a DMA command to the DMAC to setup the necessary sandboxes. The sandboxes are exclusive areas in the DRAM that only a specific attached processing unit can access).

Lee teaches of a size of the data blocks equaling a size of registers of the available secondary processor (fig. 3b; column 5, lines 20 – 40; where a block transfer

on a single register file in the computational unit, the data block can be a full register file).

It would have been obvious to one of ordinary skill in the art having the teachings of Suzuoki, the applicant's admission, Pfleiger, Hammond, and Lee at the time of the invention to make the data blocks in the DRAM of Suzuoki the same size of the APU registers in Suzuoki just like the data blocks in Lee that are the same size as a full register file in the computation unit in Lee. The motivation for this would have been to reduce the complexity and reduce the amount of overhead on the hardware, Lee column 5, lines 32 – 40.

27. With respect to claim 16, Suzuoki teaches of wherein the one first processor is further adapted to divide the common memory into data blocks (figs. 2, 24; item 2412; column 3, lines 43 – 53; column 7, lines 43 – 56; column 18, lines 32 – 35; where the processing unit allocates space in the DRAM for executing the apulet by issuing a DMA command to the DMAC to setup the necessary sandboxes. The sandboxes are exclusive areas in the DRAM that only a specific attached processing unit can access).

Lee teaches of a size of the data blocks equaling a size of registers of one of the secondary processors (fig. 3b; column 5, lines 20 – 40; where a block transfer on a single register file in the computational unit, the data block can be a full register file).

28. With respect to claim 25, Suzuoki teaches of wherein the means for dividing comprises means for dividing the common memory into data blocks (figs. 2, 24; item 2412; column 3, lines 43 – 53; column 7, lines 43 – 56; column 18, lines 32 – 35; where the processing unit allocates space in the DRAM for executing the apulet by issuing a

DMA command to the DMAC to setup the necessary sandboxes. The sandboxes are exclusive areas in the DRAM that only a specific attached processing unit can access).

Lee teaches of a size of the data blocks equaling a size of registers of the secondary processors (fig. 3b; column 5, lines 20 – 40; where a block transfer on a single register file in the computational unit, the data block can be a full register file).

29. Claims 9, 18, and 27 rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuoki and the applicant's admitted prior art Pfleiger and Hammond as applied to claims 1, 10, and 19 respectively, and further in view of Proch et al., U.S. Patent No. 6,381,659 (hereinafter Proch).

30. With respect to claim 9, Suzuoki teaches of identifying, using one of the first processors, additional available secondary processors to process data blocks (figs. 24 – 26B; item 2410; column 7, lines 57 – 66; column 18, lines 31 – 32; column 19, line 38 – column 20, line 52; where the processing unit designates an attached processing unit to process the apulet. Also where the PU assigns 3 different APUs to process a network apulet and MPEG apulets).

Proch teaches of processing the data blocks until all the data blocks have been processed (column 5, lines 28 – 39; where the first data block is read. Then the second data block is read. This is repeated until all the data blocks in the buffer have been read).

It would have been obvious to one of ordinary skill in the art having the teachings of Suzuoki, the applicant's admission and Pfleiger, Hammond, and Proch at the time of the invention to incorporate the process/concept of processing data block until there are

no more data blocks to process from Proch into the PU sorting out data blocks to the APUs in The combination of Suzuoki and the applicant's admission, Pfleiger, and Hammond. The motivation for this would have been to allow for all of the data to be processed.

31. With respect to claim 18, Suzuoki teaches of wherein one the first processors is adapted to identify additional available secondary processors to process data blocks (figs. 24 – 26B; item 2410; column 7, lines 57 – 66; column 18, lines 31 – 32; column 19, line 38 – column 20, line 52; where the processing unit designates an attached processing unit to process the apulet. Also where the PU assigns 3 different APUs to process a network apulet and MPEG apulets).

Proch teaches of processing the data blocks until all the data blocks have been processed (column 5, lines 28 – 39; where the first data block is read. Then the second data block is read. This is repeated until all the data blocks in the buffer have been read).

32. With respect to claim 27, Suzuoki teaches of means for identifying additional available secondary processors to process data blocks (figs. 24 – 26B; item 2410; column 7, lines 57 – 66; column 18, lines 31 – 32; column 19, line 38 – column 20, line 52; where the processing unit designates an attached processing unit to process the apulet. Also where the PU assigns 3 different APUs to process a network apulet and MPEG apulets).

Proch teaches of processing the data blocks until all the data blocks have been processed (column 5, lines 28 – 39; where the first data block is read. Then the second

data block is read. This is repeated until all the data blocks in the buffer have been read).

33. Additionally, claims 1 – 6, 10-15 and 19-24 rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuoki at al U.S. Patent No. 6,526,491 (hereinafter Suzuoki), an admission of prior art by the applicant and Guttag, et al., US patent 5560030 and Hammond.

34. With respect to claims, 1, 10, and 19, the combination of Suzuoki and the applicant's prior art admission and Hammond teach of the limitations cited above. Guttag teaches of processing the data block further using one of the first processors (column 13, line 25-28).

It would have been obvious to one of ordinary skill in the art having the teachings of Suzuoki, and applicants admission and Guttag at the time of the invention interpret the results of processing with the main processor (PU) as taught in Guttag. Their motivation would have been to provide a single overall result.

35. With respect to claims 2 – 6, 11-15 and 20-24, they are rejected as previously cited in paragraphs 9-13, 15-19, and 21-25 respectively.

36. Claims 7, 16, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuoki, the applicant's admitted prior art, Hammond and Guttag as applied to claims 1, 10, and 19 respectively, and further in view of Lee et al., U.S. Patent No. 6,128,724 (hereinafter Lee).

37. With respect to claims 7, 16, and 25 they are rejected as previously cited in paragraphs 27-29.

38. Claims 9, 18, and 27 rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuoki and the applicant's admitted prior art, Hammond and Guttag as applied to claims 1, 10, and 19 respectively, and further in view of Proch et al., U.S. Patent No. 6,381,659 (hereinafter Proch).

39. With respect to claims 9, 18, and 27 they are rejected as previously cited in paragraphs 31-33.

### *Response to Arguments*

40. Applicant's arguments with respect to claims 1-7, 9-16, 18-25, 27 have been considered but are moot in view of the new ground(s) of rejection.

### *Conclusion*

41. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

42. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

43. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

44. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Krofcheck whose telephone number is 571-272-8193. The examiner can normally be reached on Monday - Friday.

45. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

46. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michael Krofcheck

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